1. (Amended) A resistive structure, integrated in a semiconductor substrate, comprising: a trench having a depth greater than a width and lined with dielectric material to form a dielectric trench and a polysilicon region, at least a portion of which is doped, the polysilicon region completely surrounded by the dielectric trench, so that the resistive structure is isolated electrically from other components jointly integrated in the semiconductor substrate.

2. (Amended) The resistive structure of claim 1, wherein portions of the dielectric trench are formed with a plurality of trenches distributed about the polysilicon region to form a single dielectric region having a width that increases along the resistive structure in which a voltage drop increases.

3. (Amended) The resistive structure of claim 1, wherein said polysilicon region and said dielectric region have a serpentine pattern, thereby reducing the space requirements of the resistive structure for a given resistance value.

4. (Amended) The resistive structure of claim 3, wherein said serpentine pattern is formed to include rungs, said rungs are physically connected in parallel together by a metallization.

7. (Amended) The resistive structure of claim 1, wherein said polysilicon region comprises two deposited layers of polysilicon, only a first of said layers being enhanced by implantation to lower the values of parasitic capacitances associated with the resistive structure.

10. (Amended) The resistive structure of claim 1, wherein said dielectric region that is arranged to isolate the resistive structure is formed in the process of oxidizing the sidewalls of the dielectric trench.

11. (Amended) An integrated resistive structure, comprising:

at least one trench having a depth greater than a width formed in a semiconductor substrate;

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a dielectric layer entirely coating all walls of the at least one trench; and

a polysilicon region filling the at least one trench to be isolated dielectrically from the semiconductor substrate, the polysilicon region having at least a portion that is doped.

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19. (New) A resistive structure, integrated in a semiconductor substrate, comprising:

a trench having a depth greater than a width and lined with dielectric material to form a dielectric trench, the dielectric trench formed with a plurality of trenches distributed to form a single dielectric region having a width that increases along the resistive structure where a voltage drop increases; and

a polysilicon region, at least a portion of which is doped, filling the dielectric trench to be surrounded by the dielectric material.

20. (New) A resistive structure, integrated in a semiconductor substrate, comprising:

a trench having a depth greater than a width and aligned with dielectric material to form a dielectric trench, the dielectric trench formed with a plurality of trenches distributed to form a single dielectric region having a width that increases along the resistive structure where a voltage drop increases; and

a polysilicon region filling the dielectric trench to be surrounded by the dielectric material, the polysilicon region comprising two deposited layers of polysilicon, only a first of the layers enhanced by implantation to lower the values of parasitic capacitances associated with the resistive structure.

REMARKS

Claims 1-4, 7, 8, 10, 11, 15, 16, and 18-20 are presented for further examination. Claims 1-4, 7, 10, and 11 have been amended. Claims 19 and 20 are new.

In the Office Action mailed November 6, 2002, the Examiner objected to the drawings because metalization 101 in Figure 9 should be numbered 95. Applicants are submitting herewith new formal Figure 9, along with a marked up copy of Figure 9 showing the